DATA SHEET

AAT4687-1: Over-Voltage Protection Switch

Applications

- Cell phones
- Digital still cameras
- GPS
- MP3 players
- Personal data assistants (PDAs)
- USB hot-swap/live-insertion devices

Features

- Input voltage range up to 28 V
- Over-voltage protection threshold:
  - 5.9 V typical
  - 6 V maximum
- Fixed over-voltage protection threshold
- 2 V typical under-voltage lockout threshold
- Fast OVP response:
  - 0.7 μs typical to over-voltage transient
- Low operation quiescent current:
  - 45 μA typical
  - 1 μA maximum in shutdown (disabled)
- Thermal shutdown protection
- 120 mΩ typical (140 mΩ Max.) $R_{DS(ON)}$ at 5 V
- OVP, OTP fault indicator
- 1.8 A maximum continuous current
- Temperature range: –40 °C to +85 °C
- SC70JW (10-pin, 2.2 mm × 2.0 mm) package (MSL1, 260 ºC per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Description

The AAT4687-1 OVPSwitch™ is a P-channel MOSFET power switch with precise over-voltage protection control, designed to protect low-voltage systems against high-voltage faults up to +28 V. If the input voltage exceeds the fixed over-voltage threshold, the P-channel MOSFET switch is turned off to prevent the output load circuits from damage. The AAT4687-1 is available with an internally programmed over-voltage trip point.

The AAT4687-1 includes an under-voltage lockout (UVLO) protection circuit, which puts the device into sleep mode at low input voltages, consuming less than 1 μA of current. The AAT4687-1 also includes an enable pin ($\overline{EN}$) to enable or disable the device and an over-voltage protection (OVP), over-temperature protection ($\overline{OTP}$) fault indicator (FLT).

The AAT4687-1 is offered in a small 10-pin, 2.2 mm × 2.0 mm SC70JW package, and is specified for operation over the –40 °C to +85 °C ambient temperature range.

A typical application circuit is shown in Figure 1. The pin configuration is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

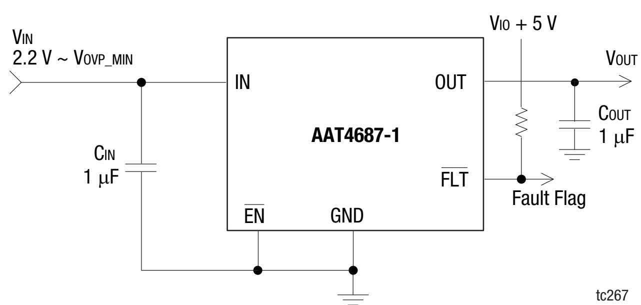

Figure 1. AAT4687-1 Typical Application Circuit

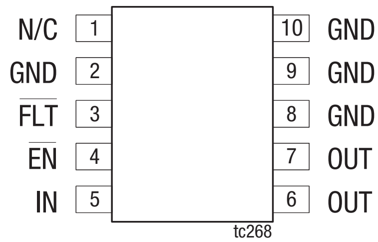

Figure 2. AAT4687-1 Pinout – 10-Pin, 2.2 mm × 2.0 mm SC70JW (Top View)

Table 1. AAT4687-1 Signal Descriptions

Pin Number	Name	Description
1	N/C	No connect.
2, 8, 9, 10	GND	Ground connection pin.
3	$\overline{\text{FLT}}$	Over-voltage or over-temperature fault reporting output pin. Open drain. $\overline{\text{FLT}}$ goes low when input voltage exceeds the over-voltage threshold or an over-temperature fault occurs. An external pull-up resistor to V_{IO} (6.5 V max) should be added.
4	$\overline{\text{EN}}$	Enable input pin, active low. An internal pull-down resistor is connected on this pin. Connect to ground for normal operation. Connect to high (6.5 V Max) to shut down the device, which then draws less than 1 μA of current.
5	IN	Power input pin. Connect 1 μF capacitor from IN to GND.
6, 7	OUT	Output. Connect a 0.1 μF ~ 47 μF capacitor from OUT to GND.

Electrical and Mechanical Specifications

The absolute maximum ratings of the AAT4687-1 are provided in Table 2, the thermal information is listed in Table 3, and electrical specifications are provided in Table 4.

Typical performance characteristics of the AAT4687-1 are shown in Figures 3 through 19.

Table 2. AAT4687-1 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
IN to GND	V_{IN}	–0.3	+30	V
OVP to GND	V_{OVP}	–0.3	+6.5	V
$\overline{\text{FLT}}$, $\overline{\text{EN}}$ to GND	V_{FLT}, V_{EN}	–0.3	+6.5	V
OUT to GND	V_{OUT}	–0.3	V_{IN} + 0.3	V
Maximum continuous switch current	I_{MAX}		1.8	A
Operating junction temperature range	T_J	–40	150	ºC
Storage temperature	T_{STG}	–40	150	ºC
Maximum soldering temperature (at leads)	T_{LEAD}		300	ºC

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed may result in permanent damage to the device.

Table 3. AAT4687-1 Thermal Information

Parameter	Symbol	Value	Units
Maximum thermal resistance (Note 1)	θ_{JA}	160	ºC/W
Maximum power dissipation (Note 1, Note 2)	P_D	625	mW

Note 1: Mounted on an FR4 board.

Note 2: Derate 6.25 mW/°C above 25 °C.

CAUTION: *Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 4. AAT4687-1 Electrical Specifications (Note 1)
(V_{IN} = 5 V, T_A = –40 °C to +85°C, Unless Otherwise Noted, Typical Values are T_A = +25 °C)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Input over-voltage protection range	V_{IN_MAX}				28	V
Normal operating input voltage range	V_{IN}		2.2		V_{OVP_MIN}	V
Operation quiescent current	I_Q	V_{IN} = 5 V, $\overline{EN}$ = 0 V, I_{OUT} = 0 A		35	60	μA
Shutdown supply current	$I_{SD(OFF)}$	$\overline{EN}$ = V_{IN}, V_{IN} = 5.5 V, V_{OUT} = 0 V			1	μA
Under-voltage lockout threshold	V_{UVLO}	Rising edge		2.0	2.2	V
Under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			0.1		V
Over-voltage lockout threshold, IN pin	V_{OVPT}	Rising edge	5.7	5.9	6	V
Over-voltage lockout threshold hysteresis, IN pin	V_{OVP_HYS}			0.15		V
MOSFET Switch						
PMOS On-resistance	$R_{DS(ON)}$	I_{OUT} = 1500 mA (Note 2), T_A = +25 °C		120	140	mΩ
Switch Off-leakage	$I_{D(OFF)}$	$\overline{EN}$ = V_{IN}			1	μA
Logic						
$\overline{EN}$ input low voltage	$V_{EN(L)}$				0.4	V
$\overline{EN}$ input high voltage	$V_{EN(H)}$		1.6			V
$\overline{EN}$ input leakage	I_{EN}	V_{EN} = 5.5 V or 0 V		0.5	2.0	μA
$\overline{FLT}$ output voltage low	$\overline{FLT}_{OL}$	I_{FLT} = 1 mA			0.4	V
$\overline{FLT}$ output leakage current	$\overline{FLT}_{IOL}$				1	μA
Timing						
$\overline{FLT}$ blanking time	t_{BLK_FLT}	From de-assertion of 0 V	5	10	15	ms
$\overline{FLT}$ assertion delay time from over-voltage (OV)	t_{D_FLT}	From assertion of 0 V		1		μs
Over-voltage release time	t_{RLS_OV}	V_{IN} fall from (6 V + TBD) to (V_{OVP_MIN} – TBD)	5	10	15	ms
Over-voltage response time	t_{RESP_OV}	V_{IN} rise from (V_{OVP_MIN} – TBD) to (6 V + TBD)		0.7		μs
Turn-on delay time	t_{ON}	V_{IN} = 5V; R_{OUT} = 10 Ω; C_{OUT} = 1 μF		10		ms
Turn-on rise time	t_R	V_{IN} = 5V; R_{OUT} = 10 Ω; C_{OUT} = 1 μF		1		ms
Turn-off delay time	t_{OFF}	V_{IN} = 5V; R_{OUT} = 10 Ω; C_{OUT} = 1 μF		9		ms
Turn-off fall time	t_F	V_{IN} = 5V; R_{OUT} = 10 Ω; C_{OUT} = 1 μF		4.5		ms
Thermal Protection						
Shutdown temperature	T_{SHDN}			150		°C
Over-temperature shutdown hysteresis	T_{HYS}			20		°C

Note 1: Performance is guaranteed only under the conditions listed in this table.

Note 2: Pulse test: pulse width = 300 μs

Typical Performance Characteristics

(V_{IN} = 5 V, T_A = –40 °C to +85°C, Unless Otherwise Noted, Typical Values are T_A = +25 °C)

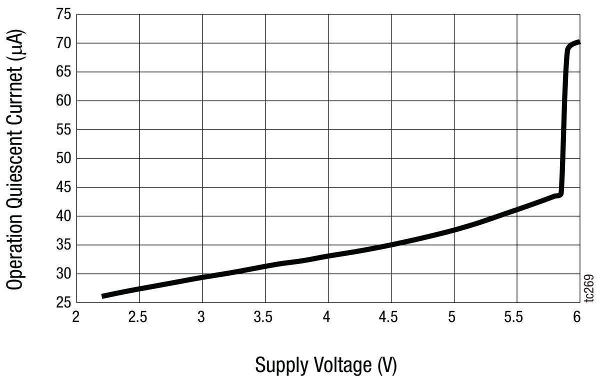

Figure 3. Operation Quiescent Current vs Supply Voltage

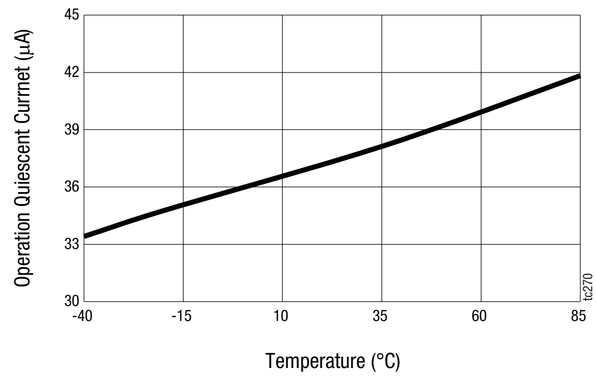

Figure 4. Operation Quiescent Current vs Temperature

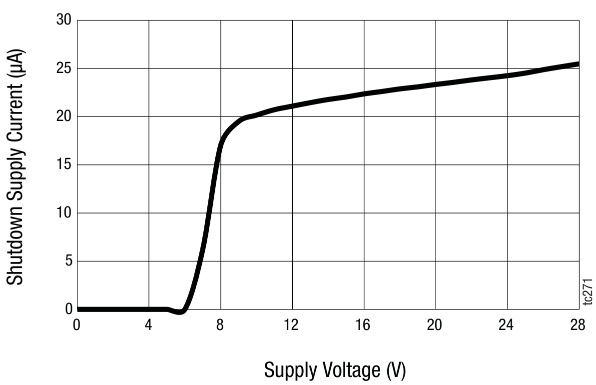

Figure 5. Shutdown Supply Current vs Supply Voltage

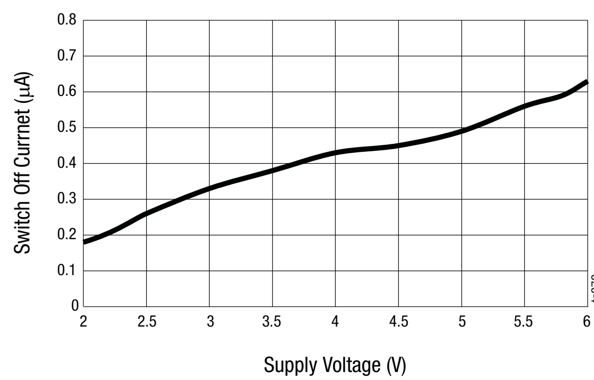

Figure 6. Switch Off Leakage vs Supply Voltage

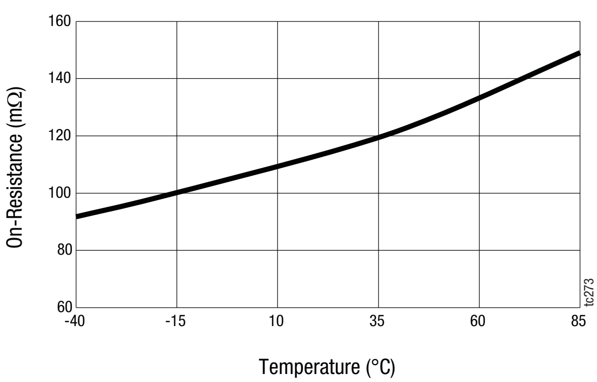

Figure 7. PMOS On-Resistance vs Temperature (V_{IN} = 5 V, I_{LOAD} = 1.5 A)

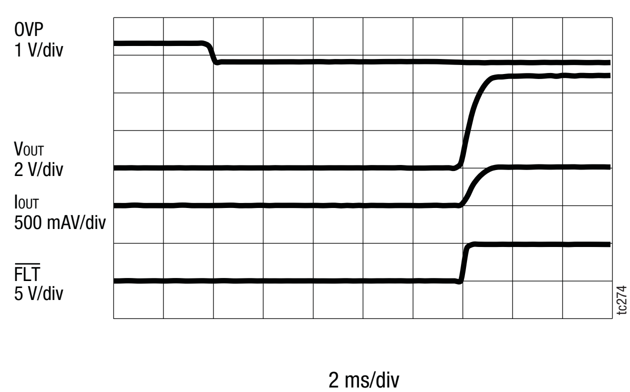

Figure 8. $\overline{FLT}$ Blanking Time (V_{IN} = 5 V)

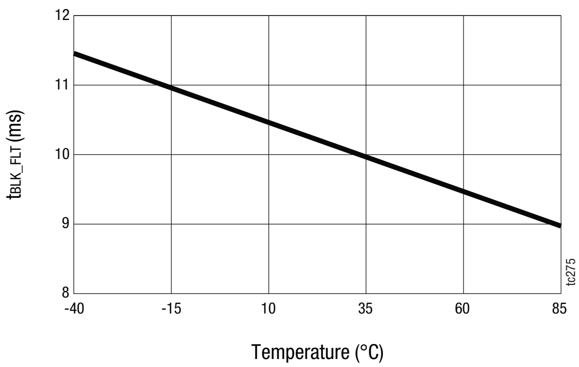

Figure 9. $\overline{\text{FLT}}$ Blanking Time vs Temperature

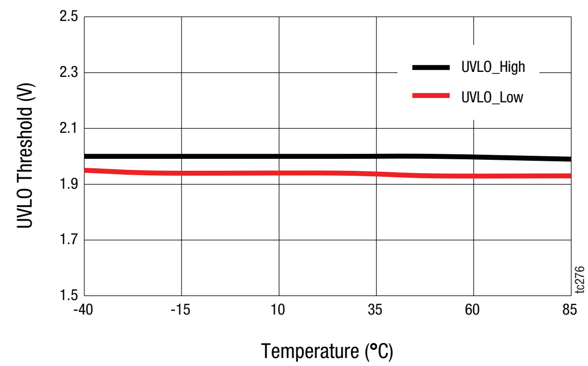

Figure 10. Under-Voltage Lockout Threshold vs Temperature

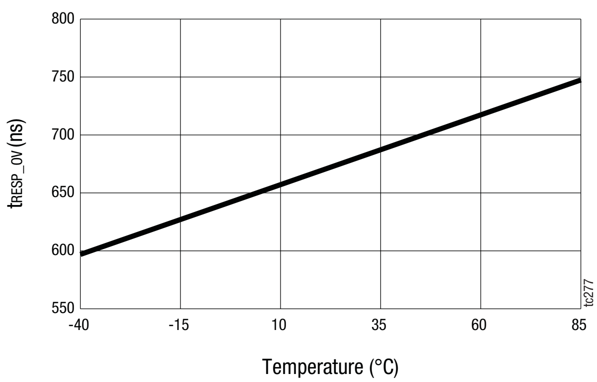

Figure 11. Over-Voltage Response Time vs Temperature

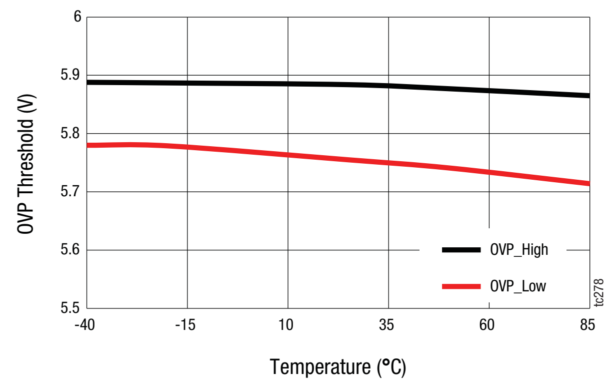

Figure 12. Over-Voltage Lockout Threshold vs Temperature

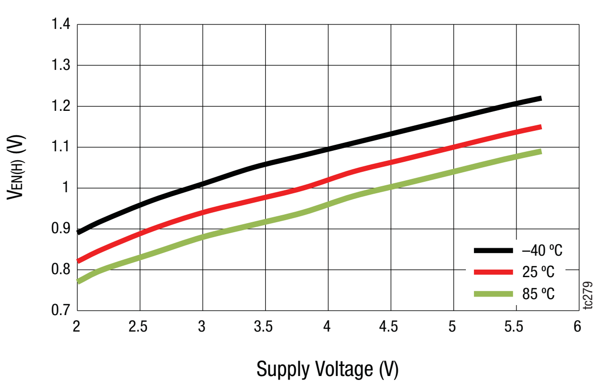

Figure 13. $\overline{\text{EN}}$ Input High Voltage vs Supply Voltage

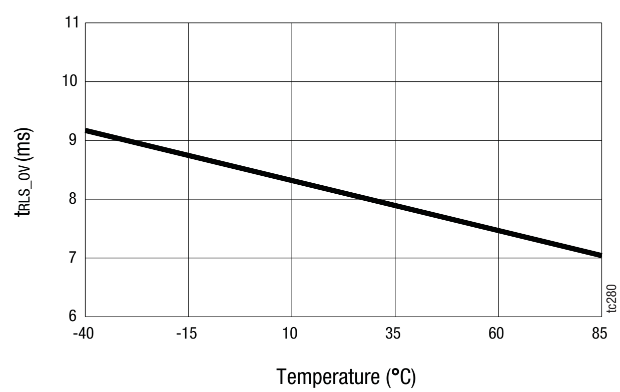

Figure 14. Over-Voltage Release Time vs Temperature

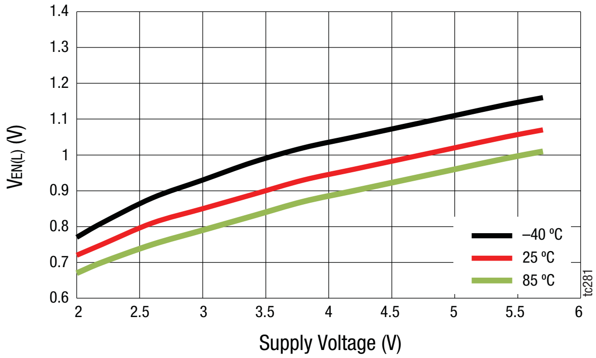

Figure 15. $\overline{EN}$ Input Low Voltage vs Supply Voltage

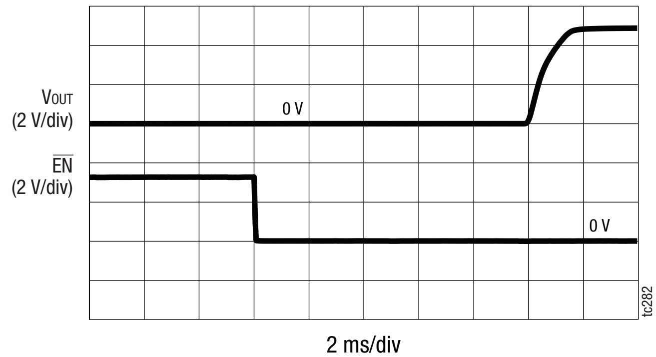

Figure 16. Turn On Delay Time (V_{IN} = 5 V, R_{OUT} = 10 Ω)

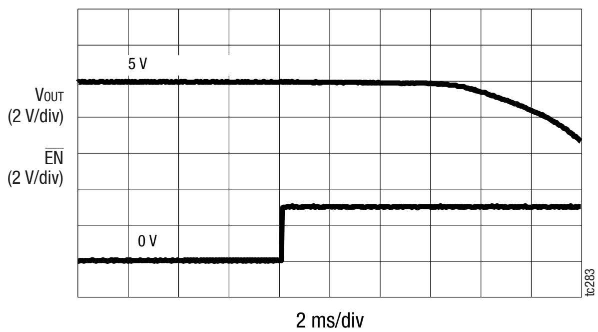

Figure 17. Turn Off Delay Time (V_{IN} = 5 V, R_{OUT} = 10 Ω)

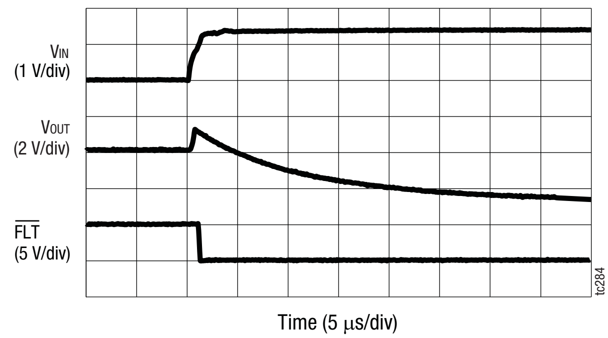

Figure 18. Over-Voltage Protection Response

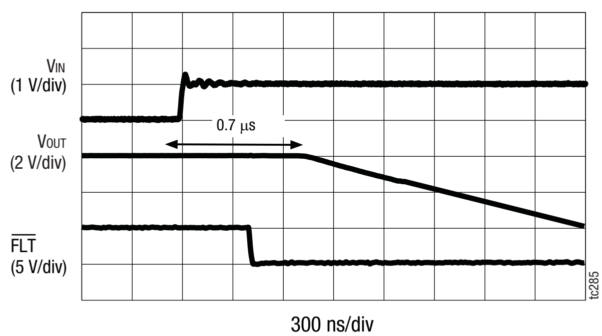

Figure 19. Over-Voltage Response Time

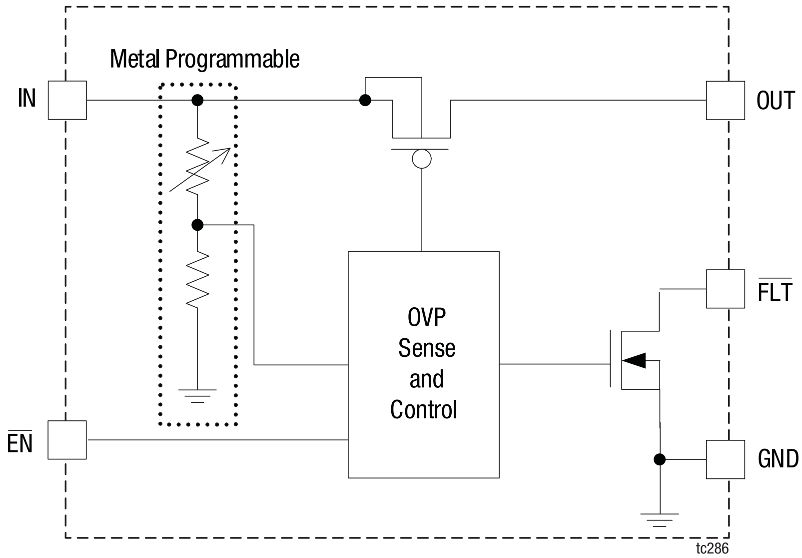

Figure 20. AAT4687-1 Functional Block Diagram

Functional Description

The AAT4687-1 provides up to 5.9 V over-voltage protection when powering low-voltage systems such as cell phones, MP3 players, and PDAs or when charging Lithium-Ion batteries from a poorly regulated supply. The AAT4687-1 is inserted between the power supply or charger source and the load to be protected. The AAT4687-1 IC includes a low resistance P-channel MOSFET, under-voltage lockout protection, over-voltage monitor, fast shutdown circuitry, and a fault output flag.

In normal operation, the P-channel MOSFET acts as a slew-rate controlled load switch, connecting and disconnecting the power supply from IN to OUT. A low resistance MOSFET is used to minimize the voltage drop between the voltage source and the load and to reduce power dissipation. When the voltage on the input exceeds the over-voltage protection trip voltage (set internally), the device immediately turns off the internal P-channel FET, disconnecting the load from the input and preventing damage to downstream components. Simultaneously, the fault flag is raised, alerting the system to a problem.

If an over-voltage condition is applied at the time of the device enable, the switch remains OFF.

A functional block diagram is shown in Figure 20. Figure 21 shows the timing diagram.

Under-Voltage Lockout (UVLO)

The AAT4687-1 has a fixed 2.0 V under-voltage lockout level (UVLO). When the input voltage is less than the UVLO level, the MOSFET is turned off. Hysteresis of 100 mV is included to ensure circuit stability.

Over-Voltage Protection (OVP)

The AAT4687-1 has a resistor divider that is internally integrated with the input voltage trip point at 5.9 V. Once the over-voltage trip level is triggered, the PMOS switch controller turns off the PMOS in less than 0.7 μs.

Over-Temperature Protection (OTP)

If the ambient temperature of the device exceeds T_{SHDN}, the OVP switch is turned off, and the pin is driven low. The OVP switch recovers automatically when the junction temperature falls below T_{SHDN} – 20 °C.

Fault Indicator ($\overline{FLT}$)

The output is an active-low open-drain fault reporting output. A pull-up resistor should be connected from $\overline{FLT}$ to the logic I/O voltage of the host system. $\overline{FLT}$ is asserted immediately if an over-voltage or over-temperature fault occurs.

Enable Control ($\overline{EN}$)

$\overline{EN}$ is an active-low enable input. $\overline{EN}$ is driven low, connected to ground, or left floating for normal device operation. Taking $\overline{EN}$ high turns off the MOSFET. In the event of an over-voltage or UVLO condition, toggling $\overline{EN}$ does not override the fault condition, and the switch remains off.

Device Operation

On initial power-up, if $V_{IN} < V_{UVLO}$ or if $V_{OVP} > V_{OVP\_TH}$ (5.9 V), the PMOS is held off. If $V_{UVLO} < V_{IN}$, $V_{OVP} < V_{OVP\_TH}$, and $\overline{EN}$ is low, the device enters startup after a 10 ms internal delay.

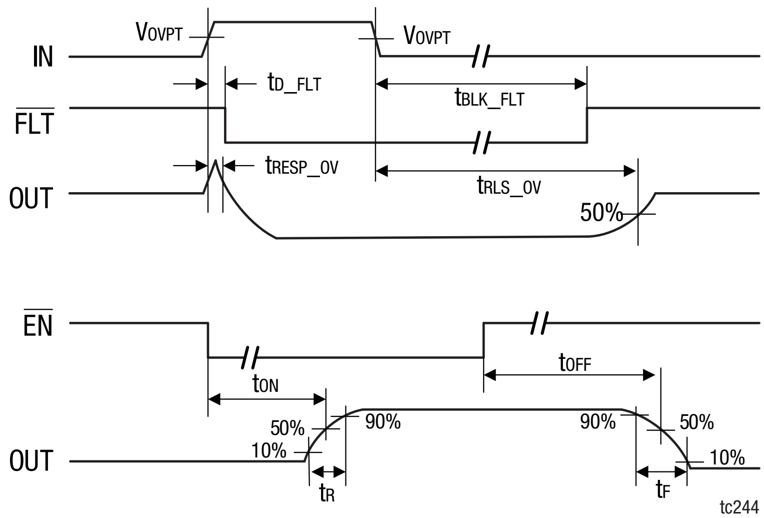

Figure 21. AAT4687-1 Timing Diagram

Application Information

Over-Voltage Protection

The AAT4687-1 over-voltage protection circuit provides fast protection against transient voltage spikes and short duration spikes of high voltage from the power supply lines. The AAT4687-1 can quickly disconnect the input supply from the load and avoid damage to sensitive components.

In portable product applications, removing the battery pack during charging can create large transients, and a high voltage spike can occur that can damage other electronic components (such as the battery charger) in the product. A "hot plug" of the AC/DC wall adapter into the AC outlet can create and release a voltage spike from the transformer. As a result, some sensitive components within the product can be damaged. With the AAT4687-1 placed between the power lines and the sensitive devices, they are insulated from the voltage spike and the input supply is disconnected in 0.7 µs.

Figure 22 shows the over-voltage protection response time test circuit.

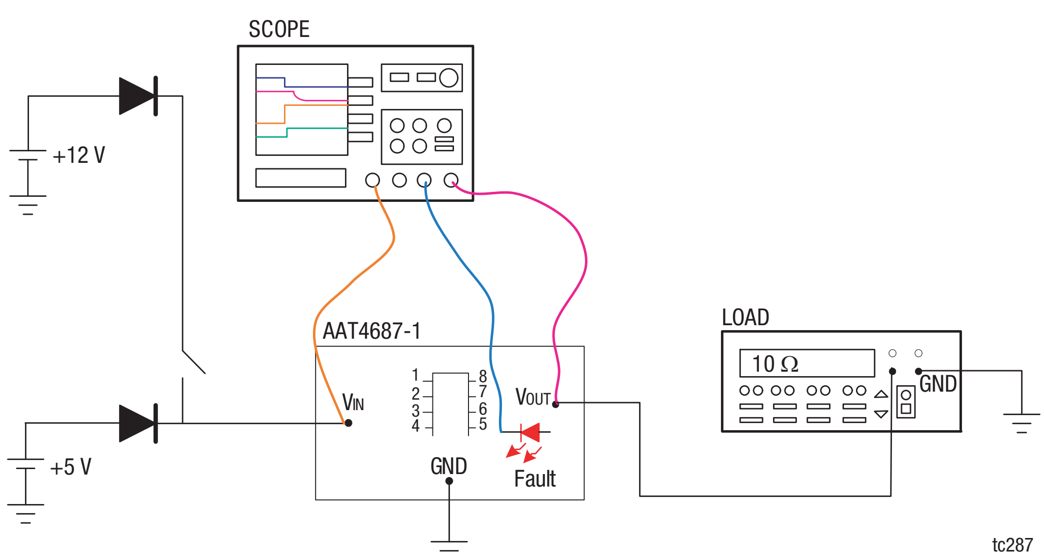

Figure 22. Over-Voltage Protection Response Time Test Circuit

Input Capacitor

A 1 μF or larger capacitor is typically recommended for C_{IN}. C_{IN} should be located as close to the device VIN pin as practically possible. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor equivalent series resistance (ESR) requirement for C_{IN}. However, for higher current operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Capacitors are typically manufactured in different voltage ratings. If the maximum possible surge voltage is known, select capacitors with a voltage rating at least 5 V higher than the maximum possible surge voltage. Otherwise, 50 V rated capacitors are generally good for most OVP applications to prevent any surge voltage.

Output Capacitor

A 0.1 μF ~ 47 μF output capacitor is required at the output. Likewise, with the output capacitor, there is no specific capacitor ESR requirement. C_{OUT} may be increased to accommodate any load transient condition.

Thermal Considerations and Maximum Output Current

The AAT4687-1 delivers a continuous output load current. The limiting characteristic for maximum safe operating output load current is package power dissipation. In order to obtain high operating currents, careful device layout and circuit operating conditions must be taken into account. The following description assumes the load switch is mounted on a printed circuit board utilizing the minimum recommended footprint as stated in the *Printed Circuit Board Layout Recommendations* section. At any given ambient temperature (T_A), the maximum package power dissipation can be determined by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

Constants for the AAT4687-1 are maximum junction temperature ($T_{J(MAX)}$ = +125 °C) and package thermal resistance (θ_{JA} = 160 °C/W). Worst-case conditions are calculated at the maximum operating temperature, T_A = +85 °C. Typical conditions are calculated under normal ambient conditions where T_A = +25 °C. At T_A = +85 °C, $P_{D(MAX)}$= 250 mW. At T_A = +25 °C, $P_{D(MAX)}$ = 625 mW.

The maximum continuous output current for the AAT4687-1 is a function of the package power dissipation and the R_{DS} of the MOSFET at $T_{J(MAX)}$. The maximum R_{DS} of the MOSFET at $T_{J(MAX)}$ is calculated by increasing the maximum room temperature.

For maximum current, refer to the following equation:

$$I_{OUT(MAX)} = \sqrt{\frac{P_{D(MAX)}}{R_{DS}}}$$

The maximum allowable output current for the AAT4687-1 is 1.8 A. If the output current exceeds 1.8 A, the device is damaged.

Printed Circuit Board Layout Recommendations

For proper thermal management and to take advantage of the low $R_{DS(ON)}$ of the AAT4687-1, certain circuit board layout rules should be followed:

- V_{IN} and V_{OUT} should be routed using wider than normal traces, and GND should be connected to a ground plane.
- To maximize package thermal dissipation and power handling capacity of the AAT4687-1 SC70JW-10 package, the ground plane area connected to the ground pins should be as large as possible.
- For best performance, C_{IN} and C_{OUT} should be placed close to the package pins.

Evaluation Board Description

The AAT4687-1 Evaluation Board is used to test the performance of the AAT4687-1. An Evaluation Board schematic diagram is provided in Figure 23. Layer details for the Evaluation Board are shown in Figure 24. The Evaluation Board has additional components for easy evaluation; the bill of materials required for the system is shown in Table 5.

Package Information

Package dimensions for the 10-pin SC70JW package are shown in Figure 25. Tape and reel dimensions are shown in Figure 26.

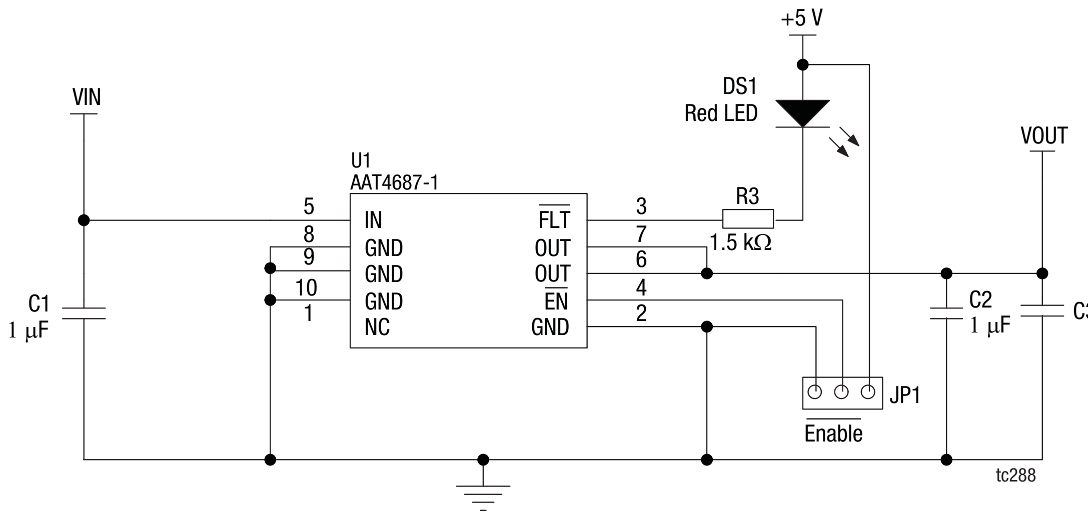

Figure 23. AAT4687-1 Evaluation Board Schematic

Table 5. AAT4687-1 Evaluation Board Bill of Materials

Component	Part number	Description	Manufacturer
U1	AAT4687-1	Over-voltage protection switch	Skyworks
R1		Not populated	
R2		Not populated	
R3	RC0603FR-071K5L	Resistor 1.5 kΩ 1/10 W 1% 0603 SMD	Yageo
C1	GRM31MR71H105K	Ceramic capacitor 1 µF 1206 X7R 50 V 10%	Murata
C2	GRM21BR71C105K	Ceramic capacitor 1 µF 0805 X7R 16 V 10%	Murata
C3		Not populated	
D1	0805KRCT	Red LED 0805	HB

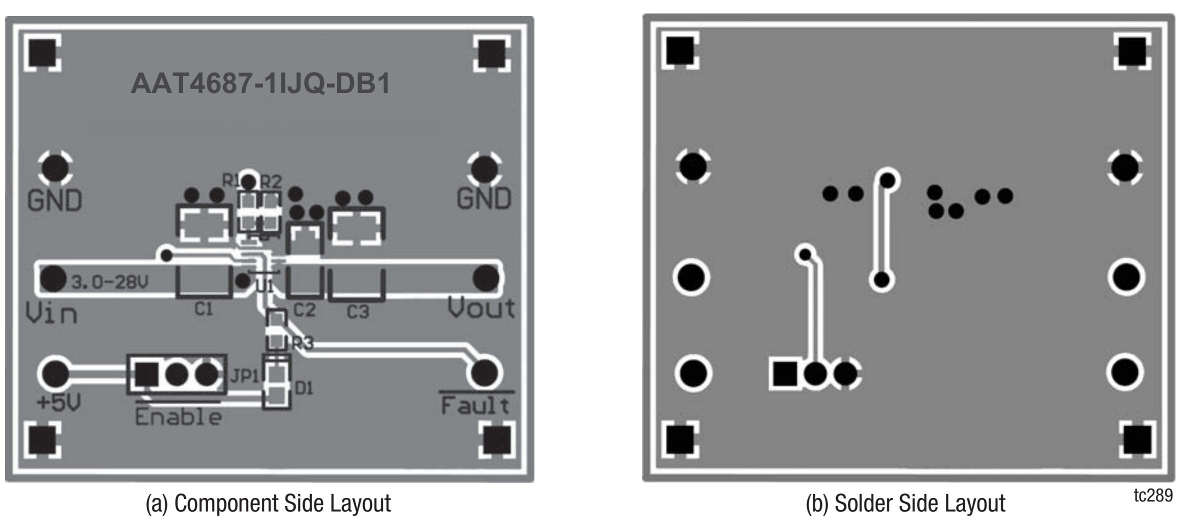

Figure 24. AAT4687-1 Evaluation Board Layer Details

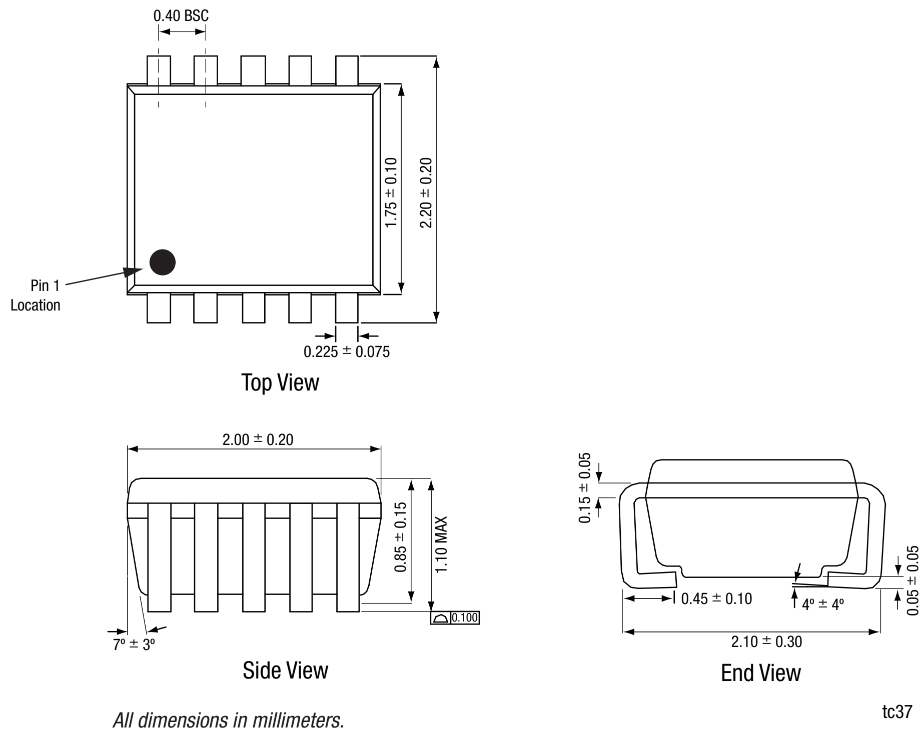

Figure 25 AAT4687-1 10-pin SC70JW Package Dimensions

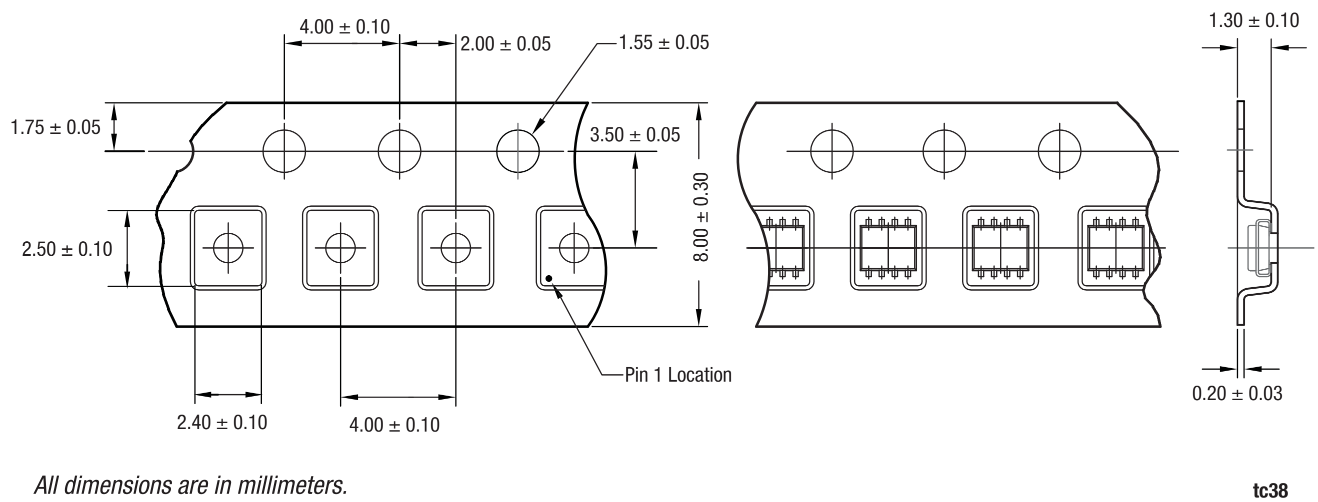

Figure 26. AAT4687-1 10-pin SC70JW Tape and Reel Dimensions

Ordering Information

Model Name	Part Marking (Note 1)	Manufacturing Part Number (Note 2)	Evaluation Board Part Number
AAT4687-1 over-voltage protection switch	U2XYY	**AAT4687-1IJQ -T1**	AAT4687-1IJQ-EVB

Note 1: XYY = assembly and date code.

Note 2: Sample stock is generally held on part numbers listed in **BOLD**.